in-plane switching mode liquid crystal display device (IPS mode LCD), where FIG. 1b is a sectional view taken along line A-A' of FIG. 1a. As shown in these figures, a gate bus line 1 and a data bus line 2 are formed on a first substrate 10, defining a pixel. Although only one pixel is drawn in the figures, the real liquid crystal liquid display device has a plurality of pixels. A common bus line 3 is aligned in the pixel, being parallel to the gate bus line 1. A thin film transistor (TFT) is disposed at the cross of the gate and data bus lines 1 and 2. As shown in FIG. 1b, the TFT comprises a gate electrode 5, a gate insulator 12, an active layer 15, and $n^+$ layer 16, a source electrode 6, and a drain electrode 7. In the pixel, a data electrode 8 and a common electrode 9 are formed parallel to the data bus line 2. A portion of the data electrode 8 which overlaps the common bus line 3 is formed to obtain a storage capacitor which functions as maintaining a grey level voltage applied into the data electrode 8. The common electrode 9 is connected to the common bus line 3. The data electrode 8 is formed on the gate insulator 12 and is connected to the drain electrode 7. The TFT, the data electrode 8 and the gate insulator 12 are covered with a passivation layer 20. Thereon, a first alignment layer 23a is coated to determine the alignment direction.

B2 cont.

**Page 4, Paragraph beginning at line 13:**

B3

An object of the present invention is to provide an in-plane switching mode liquid crystal display device wherein the aperture ratio is improved, the driving voltage is decreased, and the fabricating cost is reduced.

**Page 7, Paragraph beginning at line 19:**

B4

FIG. 1a and FIG. 1b are respectively plan and sectional views showing the conventional in-plane switching mode liquid crystal display device.

**Page 8, Paragraph beginning at line 7:**

B5

FIG. 6a and FIG. 6b are respectively plan and sectional views showing the structure of the IPS mode LCD according to the present invention.

**Page 8, Paragraph beginning at line 18:**

FIG. 10 is a plan view showing a third embodiment of the present invention.

B6 **Page 8, Paragraph beginning at line 20:**

FIG. 11a is a plan view showing a fourth embodiment of the present invention.

**Page 8, Paragraph beginning at line 24:**

B7 FIG. 12 is a plan view showing a fifth embodiment of the present invention.

**Page 10, Paragraph beginning at line 17:**

B8 The gate electrode 105, the gate bus line 101, and the common bus line 103 are formed by patterning double metal layers (Mo/Al) which is deposited by sputtering an Al layer having a thickness of 2000Å and a Mo layer having a thickness of 1000Å in the same order. The gate insulator 112 is formed thereon by depositing an inorganic insulating layer such as silicon nitride having a thickness of 4000Å by a chemical vapor deposition method. The active layer 115 and the $n^+$ layer 116 are formed by depositing and etching an amorphous silicon (a-Si) layer having a thickness of 1700Å and a $n^+$ a-Si layer having a thickness of 300Å. The data bus line 102, the data electrode 108, the source electrode 106, and the drain electrode 107 are formed by depositing and etching a Cr metal layer having a thickness of 1500Å.

**Page 14, Paragraph beginning at line 1:**

B9 drain electrodes 106 and 107. The third metal layer is formed of ITO together with the common electrode 109. In order to connect the pads to the driving circuits, it is necessary to etch the gate insulator 112 and the passivation layer 120 in the pad region. The two insulating layers in the pad region are etched when the hole 125 is formed. In the prior art, an oxide layer is generated on the pads by the exposure to the air, causing a problem that the contacting electric resistance is increased when connecting the pads to the driving circuits. However, in this embodiment, because the third metal layer of the pads is made of ITO for obtaining IOP(ITO On Passivation)

structure, the above-mentioned problem is not generated.

**Page 14, Paragraph beginning at line 14:**

B9 Cont -

FIG. 6a and FIG. 6b are plan and sectional views showing the structure of the in-plane switching mode LCD according to the present invention, where the FIG. 6b is a sectional view taken along line D-D′ of the FIG. 6a. As shown in these figures, gate and data driving circuits 150 and 154 are disposed in a frame 145 outside the display region 140. The gate and data driving circuits 150 and 154 are connected to the gate and data bus lines 101 and 102 through the gate and data pads 151 and 154 respectively. A backlight housing 147 is disposed on the upper side of the frame 145. In the backlight housing 147, a backlight 148 is disposed to project a light into a liquid crystal panel 139 through a light pipe 149. Between the light pipe 149 and the liquid crystal panel 139, a polarizer 135 is disposed to polarize the light linearly. An analyzer 136 is disposed on the front of the panel 139.

**Page 19, Paragraph beginning at line 18:**

B10

FIG. 11a, 11b, and 11c are plan and sectional views showing the fourth embodiment, where FIG. 11b and 11c are sectional views taken along lines E-E' and F-F' of FIG. 11a.

**<u>In the Claims</u>**

Please cancel claim 1 without prejudice or disclaimer.

Please add the following new claims 33-71:

Sub C1 B11

--33. (New) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;